

MMDF1N05E

Power MOSFET 1 Amp, 50 Volts

N-Channel SO-8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Features

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided
- I_{DSS} Specified at Elevated Temperature
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	50	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Drain Current – Continuous – Pulsed	I_D I_{DM}	2.0 10	A
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 2\text{ Apk}$)	E_{AS}	300	mJ
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0	W
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Temperature for Soldering, Time in Solder Bath	T_L	260 10	$^\circ\text{C}$ Sec

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

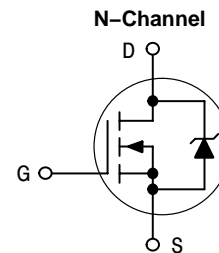
1. Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.



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1 AMPERE, 50 VOLTS
 $R_{DS(on)} = 300\text{ m}\Omega$



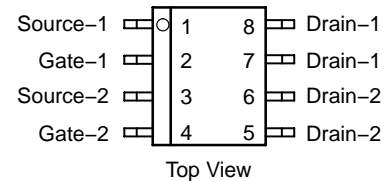
MARKING DIAGRAM



F1N05 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
MMDF1N05ER2	SO-8	2,500/Tape & Reel
MMDF1N05ER2G	SO-8 (Pb-Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMDF1N05E

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V _{GS} = 0, I _D = 250 μA)	V _{(BR)DSS}	50	–	–	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 50 V, V _{GS} = 0)	I _{DSS}	–	–	2	μA _{dc}
Gate-Body Leakage Current (V _{GS} = 20 Vdc, V _{DS} = 0)	I _{GSS}	–	–	100	nA _{dc}

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA _{dc})	V _{GS(th)}	1.0	–	3.0	Vdc
Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1.5 A _{dc}) (V _{GS} = 4.5 Vdc, I _D = 0.6 A _{dc})	R _{DS(on)} R _{DS(on)}	–	–	0.30 0.50	Ω
Forward Transconductance (V _{DS} = 15 V, I _D = 1.5 A)	g _{FS}	–	1.5	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	–	330	–	pF
Output Capacitance		C _{oss}	–	160	–	
Reverse Transfer Capacitance		C _{rss}	–	50	–	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V _{DD} = 10 V, I _D = 1.5 A, R _L = 10 Ω, V _G = 10 V, R _G = 50 Ω)	t _{d(on)}	–	–	20	ns
Rise Time		t _r	–	–	30	
Turn-Off Delay Time		t _{d(off)}	–	–	40	
Fall Time		t _f	–	–	25	
Total Gate Charge	(V _{DS} = 10 V, I _D = 1.5 A, V _{GS} = 10 V)	Q _g	–	12.5	–	nC
Gate-Source Charge		Q _{gs}	–	1.9	–	
Gate-Drain Charge		Q _{gd}	–	3.0	–	

SOURCE-DRAIN DIODE CHARACTERISTICS (T_C = 25°C)

Forward Voltage (Note 2)	(I _S = 1.5 A, V _{GS} = 0 V) (di _S /dt = 100 A/μs)	V _{SD}	–	–	1.6	V
Reverse Recovery Time		t _{rr}	–	45	–	ns

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperature.

MMDF1N05E

TYPICAL ELECTRICAL CHARACTERISTICS

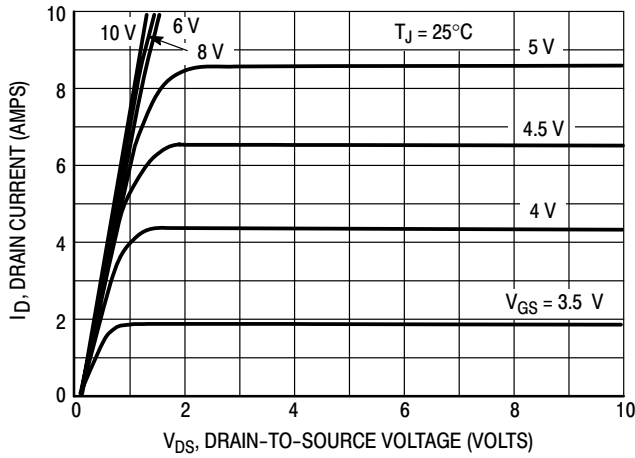


Figure 1. On-Region Characteristics

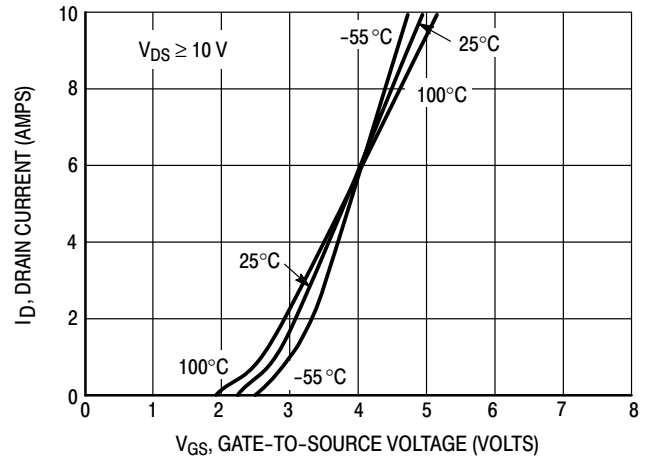


Figure 2. Transfer Characteristics

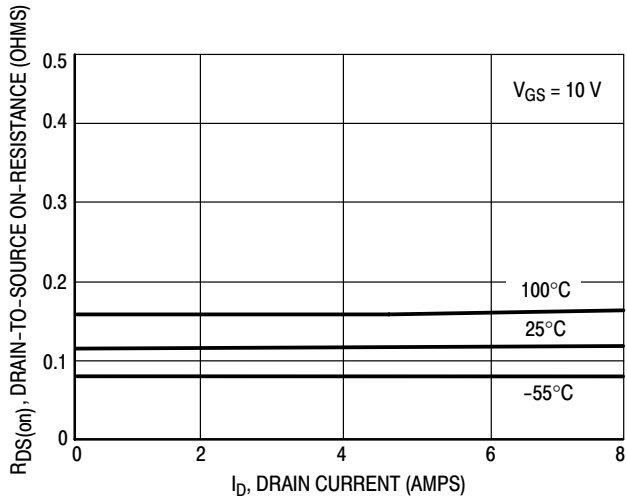


Figure 3. On-Resistance versus Drain Current

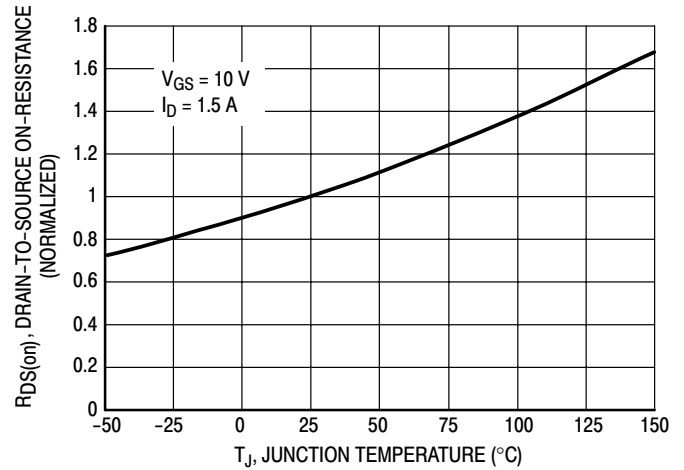


Figure 4. On-Resistance Variation with Temperature

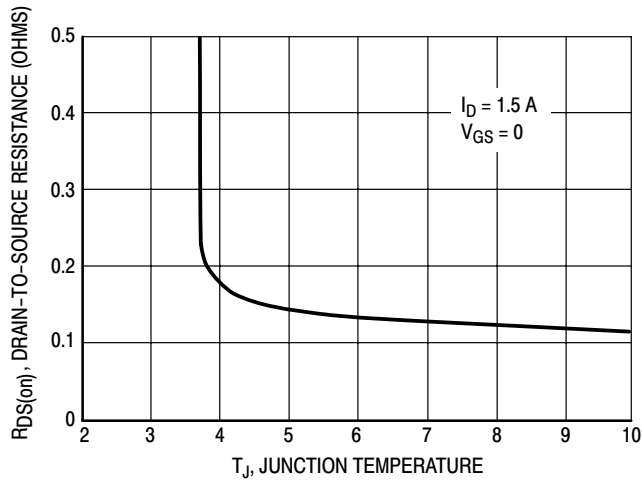


Figure 5. On Resistance versus Gate-To-Source Voltage

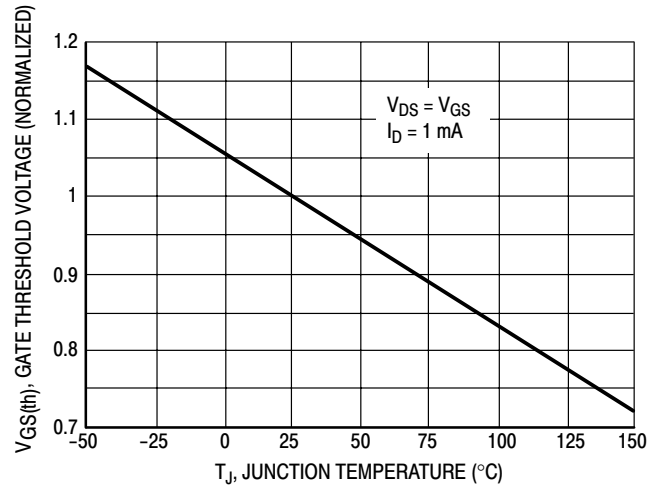


Figure 6. Gate Threshold Voltage Variation with Temperature

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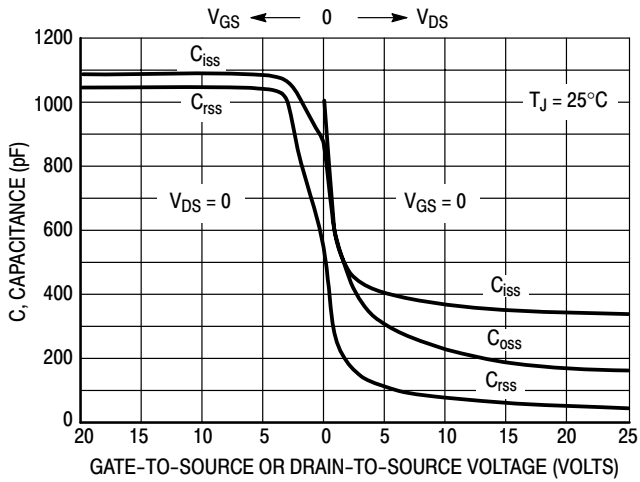


Figure 7. Capacitance Variation

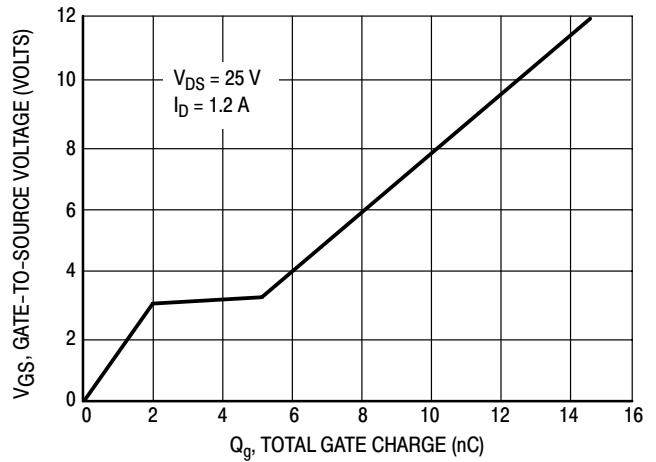


Figure 8. Gate Charge versus Gate-To-Source Voltage

SAFE OPERATING AREA INFORMATION

Forward Biased Safe Operating Area

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, "Transient Thermal Resistance – General Data and Its Use" provides detailed instructions.

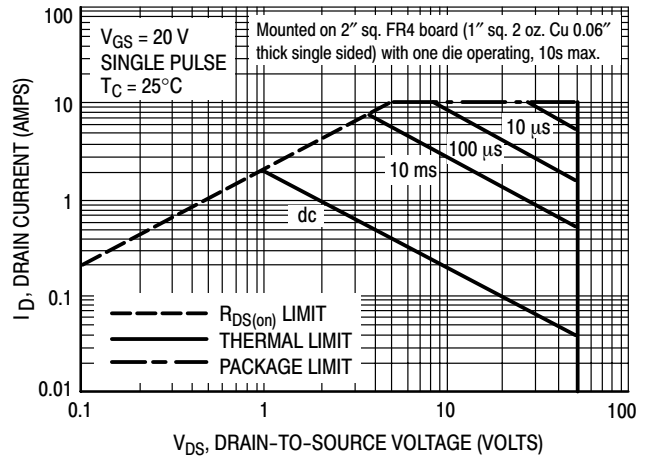


Figure 9. Maximum Rated Forward Biased Safe Operating Area

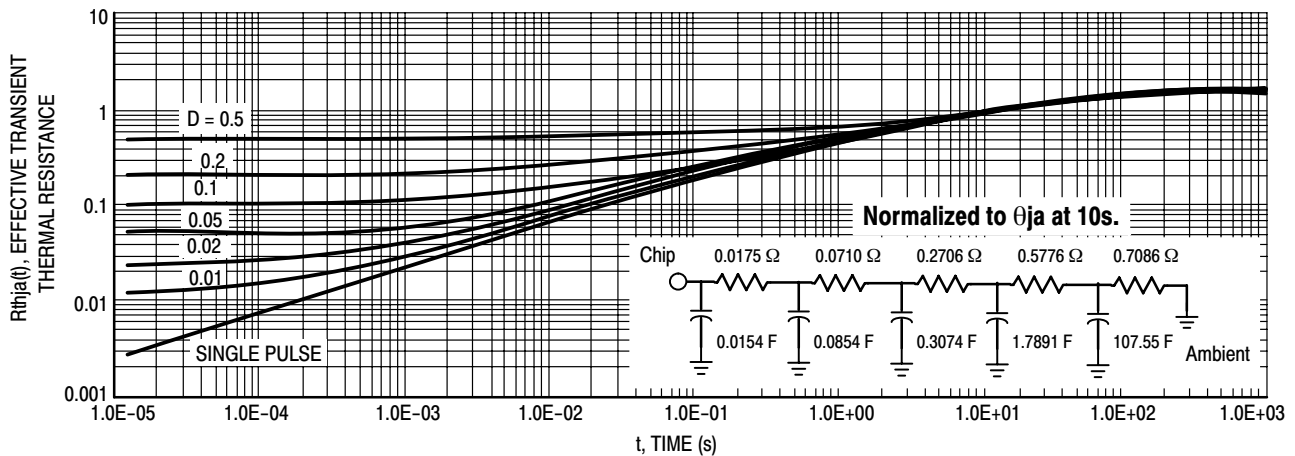
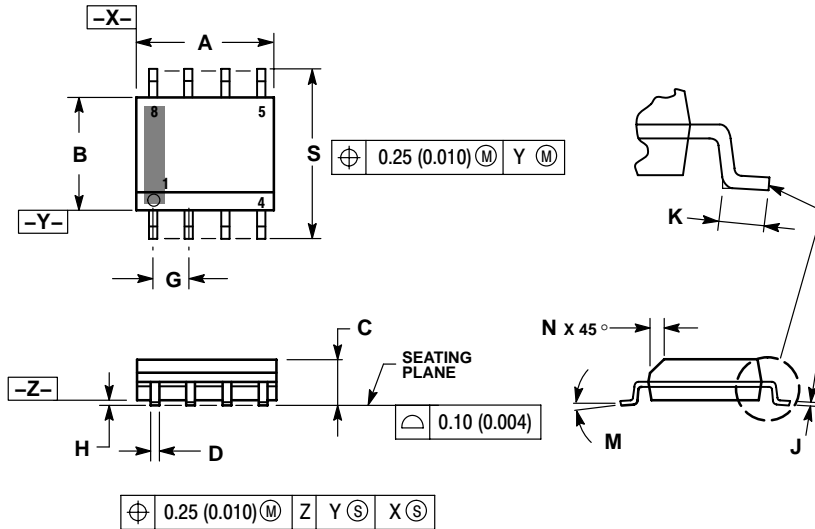


Figure 10. Thermal Response

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PACKAGE DIMENSIONS

SOIC-8
CASE 751-07
ISSUE AG



NOTES:

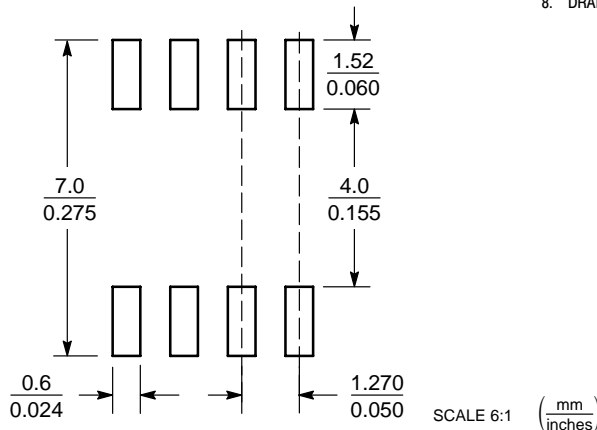
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. SOURCE 2
- 4. GATE 2
- 5. DRAIN 2
- 6. DRAIN 2
- 7. DRAIN 1
- 8. DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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